PTO/SB/33 (07-05)
United States Patent & Trademark Office; U.S. DEPARTMENT OF COMMERCE

PRE-APPEAL BRIEF REQUEST FOR REVIEW	Docket Number (Optional) 58268.00327
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on _____ Signature _____ Typed or printed Name _____	Application Number: 10/750,961 Filed: January 5, 2004 First Named Inventor: Jiann-Jyh (James) LAY Art Unit: 2113 Examiner: Yolanda L. Wilson

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a Notice of Appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ Applicant/Inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed

☒ Attorney or agent of record.
Registration No. 43,828

☐ Attorney or agent acting under 37 CFR 1.34.
Reg. No. is acting under 37 CFR 1.34 _____

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Signature

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703-720-7897
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December 18, 2006
Date

NOTE: Signatures of all of the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:
Jiann-Jyh (James) LAY
Application No.: 10/750,961
Filed: January 5, 2004

Confirmation No. 2032
Art Unit: 2113
Examiner: WILSON, Yolanda L.
Attorney Dkt. No.: 58268.00327

For: SYSTEM AND METHOD FOR SELF-ADAPTIVE REDUNDANCY CHOICE LOGIC

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

December 18, 2006

Sir:

In accordance with the Pre-Appeal Brief Conference Pilot Program guidelines set forth in the July 12, 2005 Official Gazette Notice, this is a Pre-Appeal Brief Request for Review from the final rejections set forth in an Office Action dated September 18, 2006 finally, rejecting claims 1-6, 8-16, 18 and 19. Applicants filed a Response to the Final Office Action on October 10, 2006, and the Office issued an Advisory Action dated October 23, 2006, maintaining the final rejections of claims 1-6, 8-16, 18 and 19. A Notice of Appeal is filed timely concurrently herewith. This Pre-Appeal Brief Request for Review is being timely filed to appeal the rejection of claims 1-6, 8-16, 18 and 19.

The presently pending claims are presented in the Response filed on September 18, 2006. As outlined below, no combination of the cited references discloses or suggests the elements of claims 1 and 10 and 11 and the dependent claims thereon. Claims 1-6, 10, 11, and 14-16 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,728,910 to Huang (hereinafter Huang '910). The rejection is traversed as being clearly erroneous in that the cited reference neither teaches nor suggests the novel combination of features clearly recited in independent claims 1, 10 and 11. In view of the clear error in the rejection, withdrawal thereof is respectfully requested.

Huang '910 teaches a method for self-test and self-repair of a semiconductor memory device. A single built-in self-test (BIST) engine with an extended address range is used to test the entirety of memory, i.e., both redundant and accessible memory portions, as a single array, preferably using a checkerboard bit pattern. In a first stage, faulty rows in each memory portion are identified and their addresses recorded. Known-bad rows in accessible memory are then replaced by known-good redundant rows, and the resulting repaired memory is retested in a second stage. During a second stage, repair of the accessible memory portion is verified, while defects among the redundant portion

are ignored. See at least the Abstract, Col. 3, lines 50-59 and Col. 8, line 50-Col. 9, line 19 of Huang.

Applicant submits that Huang '910 does not teach or disclose updating the redundant memory data structure to indicate that a selected redundant memory section is no longer redundant, as recited in each of Applicant's claims 1-6, 10, 11, and 14-16. Rather, Huang '910 uses the BIST test to determine bad memory locations from a memory block and then "associates" or "pairs" a good memory location in a redundant memory with the determined bad memory location from the memory block via a repair table. In Huang '910, once the association between the bad memory and the good redundant memory is finished, then the BIST re-tests the memory, and skips the bad memory locations during the test and instead tests the associated redundant memory locations in their place, as specified in the repair table. See at least Col. 3, lines 50-59 and Col. 8, line 50-Col. 9, line 19 of Huang. However, nowhere in the testing process described in Huang '910 is there any teaching or discussion of updating the redundant memory data structure to indicate that a selected redundant memory section is no longer redundant, as recited in each of the rejected claims. Col. 8, line 50-Col. 9, line 19 discloses that Huang '910 merely creates the repair table, which determines what bad memory locations in the memory block are linked to good (substitute) memory locations in the redundant memory. Nowhere in Huang '910 is the repair table described as indicating what redundant memory locations in the data structure are no longer available as redundant memory.

Further supporting Applicant's position with respect to clear error in Huang '910 is the fact the testing process of Huang '910 is disclosed therein as only being performed twice. So, according to Huang, one BIST test is conducted to determine bad memory locations, and then after the repair table and associations are created, a second BIST test is conducted to make sure that the associations function properly. If the second BIST test fails, the method of Huang '910, as disclosed in Col. 8, lines 40-45, quits and determines that the memory is faulty and not useable. On the other hand, according to the present invention as disclosed in paragraph 0024-0029 of applicant's specification, after the failed memory is replaced by a redundant memory, a second test is performed to check the redundant memory. If the redundant memory is also faulty, alternative redundant memory sections may be selected until the SRAM is determined to be functional or until all redundant memory sections have been tested. Therefore, after selection of alternative redundant memory sections, further tests are performed to determine if those memory sections are acceptable. In order to track which memory sections are currently redundant, the present invention, as recited in the present pending claims, updates the redundant memory data structure to indicate that a selected redundant memory section is no longer redundant.

Contrary to the present invention, there is no need for the testing method of Huang '910 to update a redundant memory structure to indicate that a block of the redundant memory (the block used to cover for the bad memory block location) is no longer available, as there is no third or additional testing and association step that would require further association of an available redundant memory location with a bad memory location. Given the disclosure of Huang '910, Applicants respectfully assert that the rejection under 35 U.S.C. §102(e) is in clear error and that the rejection should be withdrawn because Huang '910 does not teach or suggest each feature of claims 1, 10 and 11 and hence, dependent claims 2-6 and 14-16 thereon.

Claim 12 was rejected under 35 U.S.C. §103(a) as being obvious over Huang '910 in view of U.S. Publication No. 20020136066A1 to Huang (hereinafter Huang '066). The Office Action took the position that Huang '910 teaches each and every element recited in claim 12, except for the self adaptive logic limitations. However, the Office Action cites Huang '066 as teaching this feature. As discussed below, this rejection should be withdrawn.

Claim 13 was rejected under 35 U.S.C. §103(a) as being obvious over Huang '910 in view of U.S. Patent No. 6,993,696 Tanizaki (hereinafter Tanizaki). The Office Action took the position that Huang '910 teaches each and every element recited in claim 13, except for the state of a pin. However, the Office Action cites Tanizaki as teaching this feature. As discussed below, this rejection should be withdrawn.

Claims 8 and 18 were rejected under 35 U.S.C. §103(a) as being obvious over Huang '910 in view of U.S .Patent No. 6,181,614 Aipperspach (hereinafter Aipperspach). The Office Action took the position that Huang '910 teaches each and every element recited in claims 8 and 18, except for where the method of performed during the manufacturing process. However, the Office Action cites to Aipperspach as teaching this feature. As discussed below, this rejection should be withdrawn.

Claims 9 and 19 stand rejected under 35 U.S.C. §103(a) as being obvious over Huang '910 in view of U.S. Publication No. 20030014619A1 Cheston (hereinafter Cheston). The Office Action took the position that Huang'910 teaches each and every element recited in claims 9 and 19, except for where the method is performed during circuit power up. However, the Office Action cites to Cheston as teaching this feature. As discussed below, this rejection should be withdrawn.

All of the rejections under 35 U.S.C. 103(a) are traversed as being clearly erroneous in that the cited references neither teach nor suggest the novel combination of features clearly recited in independent claims 1 and 11, upon which each of claims 8, 9, 12, 13, 18 and 19 depend.

Huang '910 is discussed above. Huang '066 teaches a system and method for a self-repairing memory that can be integrated with any BIST mechanism, without extensive modification

to either the BIST or BISR mechanisms. A BISR "Wrapper" system interfaces the BIST engine to the BISR repair circuitry. The BISR Wrapper makes use of standard status signals present in any BIST engine, and directs the operation of the BISR circuitry. With the Wrapper, BISR operation need no longer be closely coupled to the operation or internal structure of the BIST. Consequently, modification of the BIST mechanism, e.g., to improve fault coverage, can be implemented without influencing the BISR. See at least the Abstract of Huang '066.

Tanizaki teaches a semiconductor memory device with a built-in self test circuit includes a semiconductor substrate, a memory cell array formed on the semiconductor substrate, an input buffer provided on the semiconductor substrate to receive externally applied data, a test circuit coupled to the memory cell array and the input buffer on the semiconductor substrate to store a program received through the input buffer to generate test data of the memory cell array according to the stored program to carry out testing of the memory cell array, and a select circuit selectively applying to the memory cell array test data applied from the test circuit and data applied from the input buffer depending upon a test operation and a normal operation. See at least the Abstract of Tanizaki.

Aipperspach teaches a circuit arrangement and method of dynamically repairing a redundant memory array utilize dynamically-determined repair information, generated from a memory test performed on the redundant memory array, along with persistently-stored repair information to repair the redundant memory array. In one implementation, the persistent repair information is generated during manufacture to repair manufacturing defects in the array, with the dynamic repair information generated during a power-on reset of the array to address any additional faults arising after initial manufacture and repair of the array. Furthermore, repair of dynamically-determined errors may utilize otherwise unused redundant memory cells in a redundant memory array, thus minimizing the additional circuitry required to implement dynamic repair functionality with an array. See at least the Abstract of Aipperspach.

Cheston teaches a method and system for recovering a master boot record within a data processing system. In the method, a master boot record recovery setup utility is invoked by a user. In response to invoking the master boot record recovery utility, the master boot record in a first bootable device is copied to an alternate non-volatile storage device. A recovery flag is set within BIOS indicating that the MBR has been securely copied. In response to a failed boot attempted from the first boot device, the copy of said master boot record within said alternate non-volatile storage device is accessed and utilized to boot the system. See at least the Abstract of Cheston.

Each of Huang '066, Tanizaki, Aipperspach and Cheston fails to cure the deficiencies of Huang '910, as outlined above. Specifically, each of Huang '066, Tanizaki, Aipperspach and

Cheston does not teach or suggest updating the redundant memory data structure to indicate that the selected redundant memory section is no longer redundant, as recited in claims 1 and 11, the independent claims from which claims 8, 9, 12, 13, 18 and 19 depend. Given the that disclosure of Huang '066, Tanizaki, Aipperspach or Cheston in combination with the teachings of Huang '910 fail to teach each element of claims 1 and 11, Applicant respectfully asserts that all of the rejections under 35 U.S.C. §103(a) are in clear error and that the rejections should be withdrawn because Huang '066, Tanizaki, Aipperspach or Cheston in combination with the teachings of Huang '910, do not teach or suggest each feature of claims 1 and 11, and hence, dependent claims 8, 9, 12, 13, 18 and 19 thereon.

For all of the above noted reasons, it is strongly submitted that certain clear differences exist between the present invention as claimed in claims 1-6, 8-16, 18 and 19 and the prior art relied upon by the Examiner. It is further submitted that these differences are more than sufficient that the present invention would not have been anticipated or obvious to a person having ordinary skill in the art at the time the invention was made. This final rejection being in clear error, therefore, it is respectfully requested that the Examiner's decision be reversed in this case regarding the rejections of claims 1-6, 8-16, 18 and 19, and indicate the allowability of all of pending claims 1-6, 8-16, 18 and 19. Reconsideration and withdrawal of the rejections, in view of the clear errors in the Office Action, is respectfully requested. In the event this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

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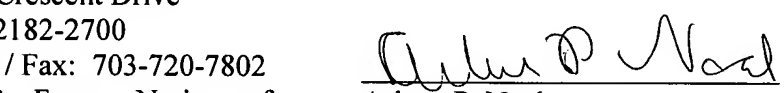
Respectfully submitted,



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